APPLICATION NOTE

Testing DDR5 Input Clock Jitter

DDR5 Electrical & Timing Measurement Techniques

KEYSIGHT

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The Big Picture

What is Clock Jitter

Clock jitter refers to the deviations in timing from a clock's ideal signal transitions. These variations are typically caused by factors such as thermal noise, fluctuations in power supply, load conditions, intrinsic device noise, and electromagnetic interference from nearby circuits. Since all DRAM command and address inputs are synchronized to the clock, the jitter must remain within the limits defined by the Joint Electron Device Engineering Council (JEDEC) to ensure reliable operation.

For load-reduced or registered DRAM modules, the clock signal is delivered via a registering clock driver. In the case of unbuffered or small-outline modules, the clock is driven either directly by the host or through a dedicated clock driver. Since clock measurements are taken within the system using a high-impedance signal capture method, a solder-in probe is employed to accurately capture the signal. To ensure precise observation, it is essential to measure the clock as close as possible to the DRAM—ideally near the termination point.

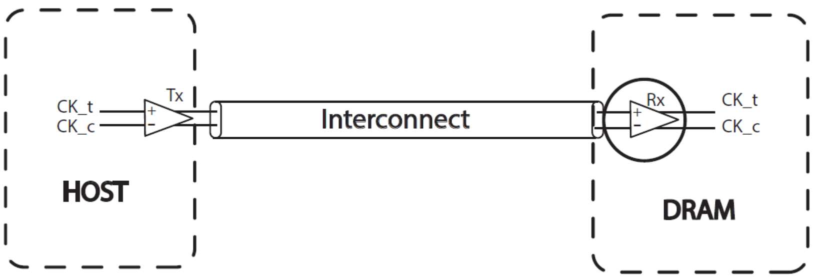

Figure 1. Input clock jitter is measured as close to the DRAM as possible.

Figure 2. A BGA interposer is used to access the clock signal, with the option to probe a backside via as well.

Sliding Analysis Window for Clock Jitter Test

Clock jitter is assessed over a sliding window spanning N unit intervals. For double data rate clocking, each unit interval includes both rising and falling edges. The accumulated jitter over N unit intervals, referred to as $T_{\text{accumulated jitter}}$ or N-UI jitter, is defined below.

$$T_{acc}^{N} = \sum_{p=m}^{m+N-1} \left(UI_p - \overline{UI}\right) \qquad m = 1,2,\dots,K-N$$

$$\overline{UI} = \frac{\sum_{p=1}^{K} UI_p}{K} \qquad p = 1,2,\dots,N,\dots K$$

For instance, a sliding analysis window of N = 1, might reference a rising edge followed by a falling edge. The next segment, N-UI2, might begin with a falling edge and then show a rising edge.

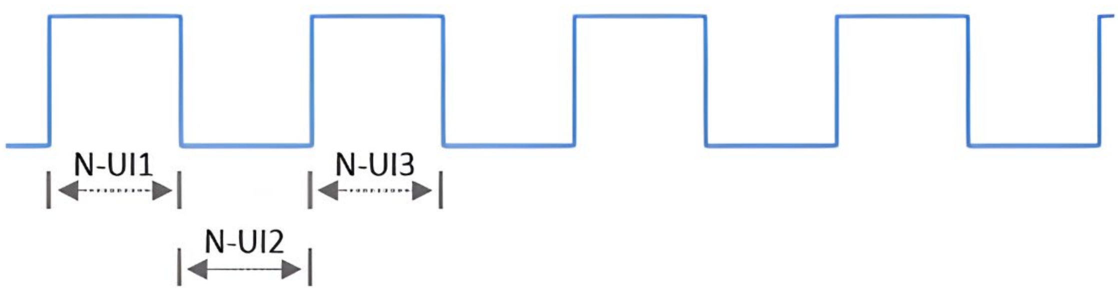

Figure 3. N-UI sliding window for N=1

With N = 4, as an example, the even number of UIs compares the same edge polarity 4 UI away across a sliding window.

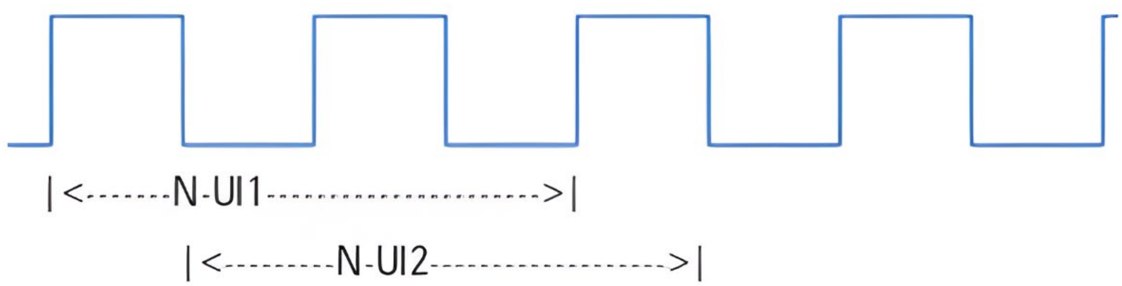

Figure 4. N-UI sliding window for N=4

Even vs. Odd Edges Matters for N-UI Jitter

N-UI jitter is defined as the time difference between a given signal edge and another edge that occurs N unit intervals later, measured relative to a known reference point. In this context, the unit interval is defined as it would be for a data waveform — meaning a clock signal is treated as a data pattern of [1 0], where the unit interval corresponds to the duration of either a '1' or a '0', effectively half the full pattern length.

In this analysis, Duty Cycle Distortion (DCD) behaves predictably:

- For even values of N, DCD is always zero.
- For odd values of N, DCD consistently yields the same non-zero value.

Here’s an example to illustrate this behavior:

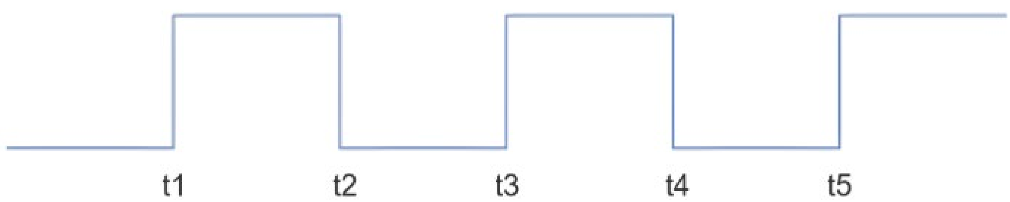

Figure 5. Even vs odd jitter: a waveform example

In N-UI jitter analysis, when N = 1, we can define jitter as follows:

- For the first rising edge: $j_1 = t_2 - t_1$
- For the first falling edge: $j_2 = t_3 - t_2$

If Duty Cycle Distortion (DCD) is present, these jitter values will differ: $j_1 \neq j_2$. As a result, the average jitter measured on rising edges will not match that of falling edges, indicating DCD > 0.

It’s important to note that this jitter measurement excludes Random Jitter (RJ). The averaging process filters out RJ effects, and since jitter is grouped by edge type (rising vs. falling), the result reflects only DCD jitter. Therefore, DCD will be non-zero for all odd values of N.

Now consider N = 2:

- For the first rising edge: $j_1 = t_3 - t_1$
- For the first falling edge: $j_2 = t_4 - t_2$

If only DCD is present, the average jitter for both rising and falling edges will be zero, and therefore DCD = 0. This holds true for all even values of N, which explains why even N-UI jitter tends to be smaller than odd N-UI jitter.

Jitter Thresholds and Specification Table Annotations

Unless stated otherwise, all jitter specifications are referenced to a Bit Error Rate (BER) of 1E-16. This is particularly important for Total Jitter (TJ) measurements, as any jitter analysis tool must be configured to use a BER level of 1E-16.

The Random Jitter (RJ) specification of 3.7 mUI can be challenging to measure accurately and consistently without considering a few key factors. As will be shown later, this low RJ limit is approaching the measurement floor of modern test equipment. To obtain a reliable RJ value, it's often necessary to subtract the oscilloscope's intrinsic RJ contribution from the measured result. Since RJ is an RMS-based parameter, this correction is performed using a Root Sum Square (RSS) subtraction calculation:

$$\text{Signal\_RJ} = \sqrt{\text{Measured\_RJ}^2 - \text{Scope\_RJ}^2}$$

The scope RJ is a function of the slew-rate based voltage noise converted to timing jitter. The formula used to calculate the effective scope RJ is based on the Period Jitter equation found in the oscilloscope's user manual. This equation accounts for the two-edge model of a clock period, which introduces the √2 factor in the calculation.

$$\text{Scope\_RJ} = \sqrt{2} \cdot \sqrt{\left(\frac{\text{Noise floor}}{\text{Slew rate}}\right)^2}$$

Effective Approaches

Probe Calibration and Deskewing

Before making measurements or even capturing signals, it's a good idea to verify the test equipment performance, specifically with probe calibration. Calibrating a solder-in probe involves two key steps: vertical calibration and skew calibration. The vertical calibration should always be performed first, followed by the skew.

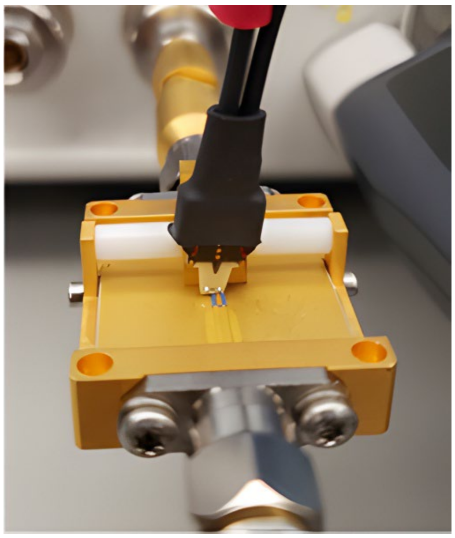

Figure 6. Example probe setup: positive lead to center conductor, negative lead to ground plane

After completing the DC gain and offset calibration, use the same setup to proceed with the skew calibration. Maintaining the same configuration ensures consistency and accuracy in the calibration process.

Removing Random Jitter

By analyzing the intrinsic instrument noise and signal slew rate, the oscilloscope can determine its internal jitter contribution and subtract it from the measured random jitter RJ.

During calibration, you'll be prompted to disconnect your probe from the oscilloscope input. However, because the probe amplifier introduces noise into the system, it should remain connected to the oscilloscope. Instead, disconnect only the probe head from the amplifier to isolate residual signal noise from the scope's internal noise.

The automatic jitter calibration process involves measuring the AC Vrms of the oscilloscope's baseline noise at the same voltage level where the jitter threshold will be set. Then, the slew rate of the data signal—between the upper and lower threshold limits — is measured during the actual jitter test. Using these two values, the oscilloscope calculates its own random jitter based on performance equations from its datasheet. This calculated RJ is then subtracted from the reported RJ and TJ. The calculated oscilloscope RJ is also included in the jitter results.

Reducing Noise with Bandwidth Limit

The measured RJ is strongly influenced by the oscilloscope's bandwidth setting. Using excessive bandwidth can introduce additional out-of-band noise and RJ. Conversely, insufficient bandwidth may result in an unrealistic test setup that doesn't reflect actual system behavior.

Since JEDEC does not specify a required oscilloscope bandwidth for clock jitter measurements, it's up to the user to select an appropriate setting. This decision should consider the bandwidth of the actual DRAM receiver (e.g., VGA bandwidth) and the frequency-dependent loss characteristics of the channel. The chosen bandwidth should also support consistent slew rate performance.

To assess the signal's high-frequency content, enable the frequency domain view. If the signal power drops below 30–40 dB at a certain frequency, that point may be suitable for limiting the bandwidth. Regardless of the bandwidth setting, always use the oscilloscope's maximum sample rate to minimize aliased noise.

Figure 7. Use the Fast Fourier Transform (FFT) view to analyze the signal's frequency content and identify the optimal bandwidth setting based on actual signal energy.

Testing DDR5 Input Clock Jitter

The following steps outline how to measure DDR5 input clock jitter using a jitter and noise analysis application in the Keysight UXR Infiniium oscilloscope software:

1. Ensure that both the oscilloscope and probe are properly calibrated before beginning the measurement. If calibration has already been performed, this step can be skipped.

2. Use an interposer or another suitable signal access method to attach the probe as close as possible to the DRAM input. Keep wire lengths to a minimum to reduce lead inductance and preserve signal integrity.

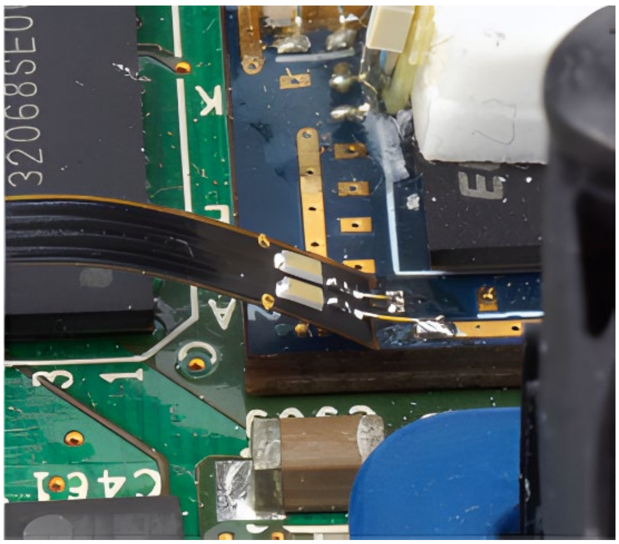

Figure 8. Probe head attached to BGA interposer

3. Power on the system to begin clock transmission. If possible, set neighboring lanes to fixed DC levels to minimize interference.

4. Adjust the oscilloscope's vertical scale and offset so the signal is centered on the screen and displayed with maximum amplitude range.

Figure 9. Optimum position of differential clock

5. Adjust the oscilloscope's time base to capture at least 1 million unit intervals. A setting of 10 µs/div or greater is recommended to ensure sufficient data for jitter analysis.

Figure 10. Capture 1 MUI with 10 µs/div minimum

6. Navigate to *Setup → Bandwidth Limit* to set the oscilloscope's bandwidth appropriately. For example, when analyzing DDR5-5600, a bandwidth setting of 10 GHz has been found to provide optimal results.

7. Navigate to *Analyze → Jitter/Noise → Advanced → Remove, Specify Jitter, Noise*. In the *Remove Scope Random Jitter* section, select *Automatic*, then click *Calibrate Scope Jitter/Noise*.
Note: If this is your first time running the calibration, you may be prompted to launch the *Jitter Wizard*. This tool helps optimize key settings such as vertical and horizontal scales, memory depth, and clock recovery parameters to ensure accurate jitter analysis.

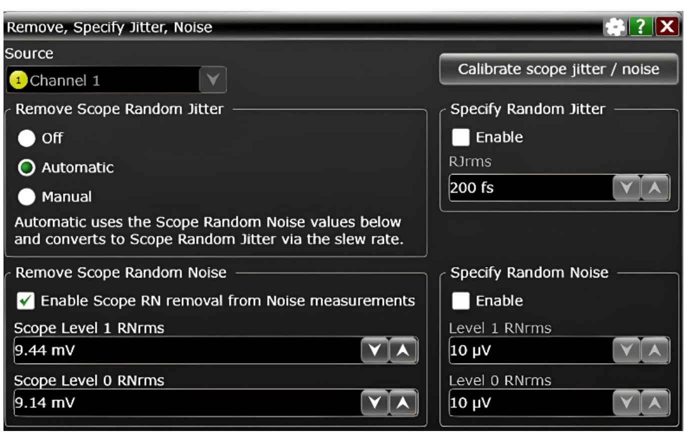

Figure 11. Settings for removal of scope random jitter

8. Detach the probe head while keeping the probe amplifier connected to the oscilloscope's channel input.

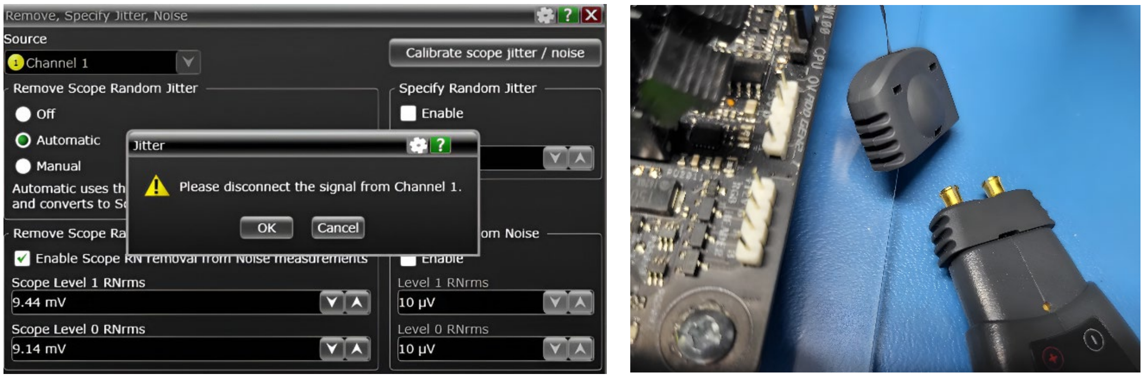

Figure 12. During noise profile calibration, the signal needs to be disconnected from the oscilloscope input. This is done by detaching the probe head, while keeping the probe amplifier connected to the scope channel.

9. Once the *Calibration Complete message* appears, reconnect the probe head to the probe amplifier.

Figure 13. Reconnect prompt after completion

10. Navigate back to Analyze → Jitter/Noise → Setup.

11. Configure the application settings:

- Set Threshold to 0 and apply appropriate hysteresis levels (use Auto if unsure).
- Set Clock Recovery to Constant Frequency.
- Set BER Level to 1E-16.
- Set Pattern Length to Period and check the Auto box.

12. Check the *Enable* box and adjust these settings:

- Under Spectral & Tail Fit, select Report Tail Fit.
- Set Display Units to Unit Interval.
- Choose Edges = Both
- Set N = 1 initially. You can incrementally advance to N = 2, 3, ...30 for deeper analysis.

Figure 14. Final EJZIT configuration

13. Click the Clear button to remove any previously generated results and waveform data.

Figure 15. Clear display

14. Click *Run* or *Single* to capture a new signal

Figure 16. Result overview with BER bathtub and histogram plots

Important Note

Duty Cycle Distortion (DCD) is present in the signal, but UDJdd does not include Bounded Uncorrelated Jitter (BUJ). This complies with DDR5 clock jitter measurement requirements, which exclude BUJ. Additionally, RJ is independent of BUJ when using Tail Fit analysis.

Total Jitter Evaluation:

Use the UTJ(1E-16) value to determine the Total Jitter (TJ) excluding BUJ.

Example results for DDR5-5600:

Random Jitter (RJ): 1-UI RMS = 11.8 mUI (2.1 ps)

Deterministic Jitter (DJ):1-UI = 29.6 mUI (5.3 ps)

Total Jitter (TJ):1-UI = 225.4 mUI (40 ps)

Key Takeaways

This app note covered the impact of clock timing variations on memory system reliability. The DDR5 standard enforces strict limits on RJ, DJ, and TJ, measured across a moving window of N unit intervals to capture short-term jitter behavior.
Accurate jitter measurement requires careful attention to probe calibration, instrument RJ removal, bandwidth control, and proper use of the jitter/noise analysis application. As demonstrated in the DDR5-5600 example, precise setup and calibration are essential for evaluating jitter levels and ensuring robust memory performance.

References

1. DDR5 DRAM Standard, JESD79-5C_V1.31,JED EC, July 2024

Frequently Asked Questions

What is the Purpose of the DDR5 Input Clock Jitter Test?

As a general overview, testing the input clock jitter will verify that the input clock (CK) meets timing and stability requirements set by JEDEC, specifically minimizing timing errors due to fluctuations (jitter) in the clock edge timing thus maintaining synchronization between the memory controller and DRAM.

What does the DDR5 Standard Require N-UI Jitter to Evaluate Clock Timing Accuracy?

N-UI is a common method to define timing from one edge to another in a clock pattern. N-UI jitter is defined as the difference between the time of an edge, and another edge N unit intervals away relative to a known reference. A clock pattern will not have any non-transition edges.

Why is DCD Always Zero for Even N-UI Jitter?

Duty Cycle Distortion (DCD) is the deviation of a clock signal's duty cycle from the ideal 50% ratio. It is typically measured as the difference in time between the high and low durations of the clock signal within a single period. For even cycles of N, the edges to be compared are the same polarity thus the difference within the same edge type would be zero.

What are Some Ways to Improve the Measurement Accuracy of Input Clock Jitter?

There are two basic methods to reduce the impact of test equipment error on the jitter measurement. First, is to reduce the oscilloscope bandwidth, thus reducing out of band noise that will increase effective measured random jitter. Second, is to characterize and remove the test equipment induced random jitter from the measurement jitter. In this way, the measurement result will represent the true signal jitter only.

What Oscilloscope Bandwidth Should be Used to Measure Clock Jitter?

Excessive bandwidth can lead to pessimistic or over report jitter results. To ensure the proper bandwidth is used, you can adjust the oscilloscope bandwidth to the point right before the measured slew rate changes. Or you can observe the frequency domain view of the signal and decrease the bandwidth to the appropriate frequency such that all signal energy below 40 or 50 dB is filtered or reduced.

Learn More

How to Test DDR5 Transmitter Compliance

How to Characterize and Test DDR5 Receiver Compliance

How to Perform DDR5 System Validation

How to Determine DDR5 Controlled Trace Impedance

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